IN THE CLAIMS:

Please amend claims 1-11, 13-18, and 20 to read as follows:

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1. (Amended) A method for improving the performance of an RF power amplifier circuit comprising:

sensing a collector current in an input stage transistor;

feeding a current equal or proportional to said input stage transistor collector current to an output stage bias circuit to boost the bias of an output stage;

wherein the input stage transistor is operated in a class AB mode, and said output stage is fed through a matching network.

2. (Amended) The method of claim 1, wherein the input stage transistor collector current is sensed and fed to the output stage bias circuit via a current mirror.

3. (Amended) The method of claim 2, wherein one transistor comprising said current mirror is connected in series with a transistor that itself forms a second current mirror with the input stage transistor.

4. (Amended) The method of claim 3, wherein the amplifier circuit comprises plural bipolar junction transistors (BJTs).

5. (Amended) The method of claim 3, wherein the amplifier circuit comprises plural field effect transistors (FETs).

6. (Amended) The method of claim 3, wherein the amplifier circuit comprises a combination of BJTs and FETs.

7. (Amended) A transistor circuit, comprising:

an input stage;

an output stage with a biasing circuit; and

a current mirror, which senses an input signal current and

feeds a current proportional to said input signal current to an output stage biasing circuit.

8. (Amended) The circuit of claim 7, wherein said current mirror includes at least one BJT.

9. (Amended) The circuit of claim 7, wherein said current mirror includes at least one FET.

10. (Amended) The circuit of claim 7, wherein transistors comprised within said circuit include both BJTs and FETs.

11. (Amended) A method of adaptively boosting the output stage bias of an amplifier circuit, comprising:

sensing an input signal; and

boosting an output stage bias with a current equal or proportional to the input signal.

12. The method of claim 11, where the input signal is an RF signal.

13. (Amended) The method of claim 12, where the input signal is sensed by a current mirror.

14. (Amended) The method of claim 13, where a collector current of an input stage BJT is mirrored by the current mirror and fed into an output stage biasing circuit.

15. (Amended) The method of claim 13, where a drain current of an input stage FET is mirrored by the current mirror and fed into an output stage biasing circuit.

16. (Amended) The method of claim 15, where the current mirror comprises BJTs.

17. (Amended) The method of claim 15, where the current mirror comprises FETs.

18. (Amended) A subcircuit, to be used in an amplification circuit, comprising:

an input sensor, arranged to sense an input signal to the amplification circuit; and

an output stage booster, arranged to boost a bias of an output stage of the amplification circuit in proportion to said input signal.

19. The subcircuit of claim 18, where the input signal is an RF signal.

20. (Amended) The subcircuit of claim 19, where the input sensor is a current mirror.

Please add new claims 21-26 as follows;

21. (New) A bias boosting subcircuit for a multi-stage power amplifier circuit, said multistage power amplifier comprising at least an input stage and an output stage, said subcircuit comprising:

two matched BJTs in a first current mirror,

wherein the first current mirror senses a collector current of an amplifying transistor in the input stage, and feeds an equal or proportional current to a bias circuit of the output stage.

22. (New) The subcircuit of claim 21, where one of the transistors of the first current mirror is connected in series with a third transistor, said third transistor itself forming a second current mirror with the input stage amplifying transistor.

23. (New) The subcircuit of claim 22, where the first current mirror comprises two matched PNP BJTs, and the second current mirror comprises two matched NPN BJTs.

24. (New) The subcircuit of claim 23, where one transistor of the first current mirror has its collector connected to a collector of said third transistor.

25. (New) The subcircuit of claim 24 comprising further transistors and wherein a collector of at least one of said further transistors is contained within said first current mirror and is connected to a collector of an NPN transistor in the output stage.

26. (New) The subcircuit of claim 25, where said output stage also comprises an NPN transistor that is itself part of a current mirror.